In the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

10. (currently amended) A fabrication method for a flash memory device, comprising:

providing a first conductive type substrate, wherein the substrate comprises a second conductive type first well region, a first conductive type second well region which is formed in and shallower than the second conductive type first well and at least a pair of stacked gate structures which are sequentially formed thereon, wherein a gap is located between the pair of stacked gate structures;

forming ~~a~~ source/~~region and a~~ drain regions in the substrate beside two sides of the stacked gate structures, wherein a first source/drain region is below the gap and a pair of second source/drain regions is outside the stacked gate structures;

forming a plurality of spacers on ~~a~~ sidewalls of the stacked gate structures;

forming a first patterned photoresist layer on the substrate, the first patterned photoresist layer exposes the gap ~~the substrate at the drain region~~;

etching the substrate ~~at the drain region~~ until penetrating through ~~the~~ a junction between the first source/drain region and the first conductive type second well region to form a first trench by using the first patterned photoresist layer and the stacked gate structures with the spacer as a masks;

removing the first patterned photoresist layer;

forming a second patterned photoresist layer on the substrate, the second patterned photoresist layer exposes a portion of the substrate outside the stacked gate structures ~~at the source region~~;

etching the portion of the substrate ~~at the source region~~ to the second conductive type first well region to form a pair of second trenches by using the

second patterned photoresist layer and the stacked gate structures with the spacers as ~~a~~masks;

performing an ion implantation process to implant dopants ~~at a~~into bottoms and ~~a~~sidewalls of the second trenches ~~on the substrate~~ to form a pair of doped regions;

removing the second patterned photoresist layer;

~~forming a first conductive layer on the substrate, wherein the first conductive layer fills spaces between and aside of the stacked gate structures~~;

~~removing a portion of the first conductive layer to~~ forming a first contact plug in the first trench ~~on the source region~~ and to form a pair of second contact plugs in the second trenches, wherein the first contact plug electrically short the first source/drain region below the gap, and the second contact plug electrically connects with the second source/drain regions disposed outside the stacked gate structures and the doped regions ~~a second conductive layer on the first conductive type second well region, wherein the first contact electrically connects with the source region and the doped region~~;

~~patterning the second conductive layer to form a second contact, wherein the drain region and the first conductive type second well region are short circuited by the second contact;~~

forming an interlayer dielectric layer on the substrate; ~~and~~

forming a third contact plug which connects with the first contact plug in the interlayer dielectric layer; and

forming a conductive line on the interlayer dielectric layer, wherein the conductive line electrically connects with the ~~second~~third contact plug.

11. (original) The method of claim 10, wherein the ion implantation process includes a tilt angle ion implantation process.

12. (currently amended) The method of claim 11, wherein ~~a~~ the tilt angle for the ion implantation process is about 15 degrees to about 30 degrees.

13. (currently amended) The method of claim 10, wherein an angle between the bottoms and the sidewalls of the second trenches ~~and the sidewall of the trench form~~ is an obtuse angle.

14. (currently amended) The method of claim 10, wherein the doped regions ~~dopants of the ion implantation process~~, the source region and the drain region are ~~the~~ doped with a same type of dopants.

15. (canceled)

16. (original) The method of claim 10, wherein the first conductive type substrate includes a P-type substrate.

17. (original) The method of claim 10, wherein the second conductive type first well region includes an N-type well region.

18. (original) The method of claim 10, wherein the first conductive type second well region includes a P-type well region.

19. (original) The method of claim 10, wherein the step of removing the first conductive layer includes performing back etching.

20. (original) The method of claim 10, wherein the step of removing the first conductive layer includes performing chemical mechanical polishing.